

Features

- High-performance and Low-power AVR[®] 8-bit RISC Architecture
 - 118 Powerful Instructions – Most Single Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Up to 8 MIPS Throughput at 8 MHz
- Data and Non-volatile Program Memory
 - 4K Bytes of In-System Programmable Flash
Endurance 1,000 Write/Erase Cycles
 - 128 Bytes of SRAM
 - 256 Bytes of In-System Programmable EEPROM
Endurance: 100,000 Write/Erase Cycles
 - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
 - One 8-bit Timer/Counter with Separate Prescaler
 - Expanded 16-bit Timer/Counter with Separate Prescaler, Compare, Capture Modes and 8-, 9-, or 10-bit PWM
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - Programmable UART
 - 6-channel, 10-bit ADC
 - Master/Slave SPI Serial Interface
- Special Microcontroller Features
 - Brown-out Reset Circuit
 - Enhanced Power-on Reset Circuit
 - Low-power Idle and Power-down Modes
- Power Consumption at 4 MHz, 3V, 25°C
 - Active: 3.4 mA
 - Idle Mode: 1.4 mA
 - Power-down Mode: <1 µA
- I/O and Packages
 - 20 Programmable I/O Lines
 - 28-lead PDIP and 32-lead TQFP
- Operating Voltage
 - 2.7V - 6.0V for the AT90LS4433
 - 4.0V - 6.0V for the AT90S4433
- Speed Grades
 - 0 - 4 MHz for the AT90LS4433
 - 0 - 8 MHz for the AT90S4433



8-bit AVR[®] Microcontroller with 4K Bytes of In-System Programmable Flash

AT90S4433
AT90LS4433

Summary

**Not Recommend for
New Designs. Use
ATmega8.**

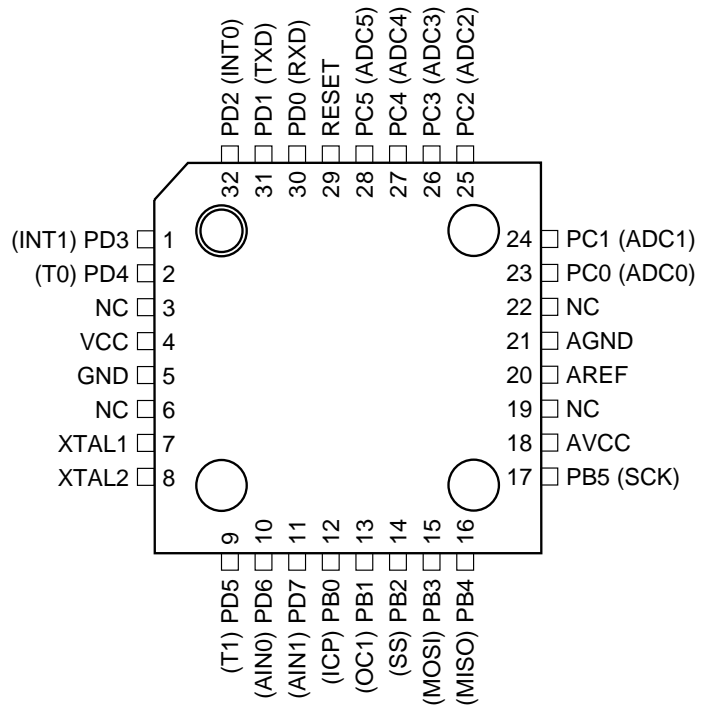
Rev. 1042HS-AVR-04/03



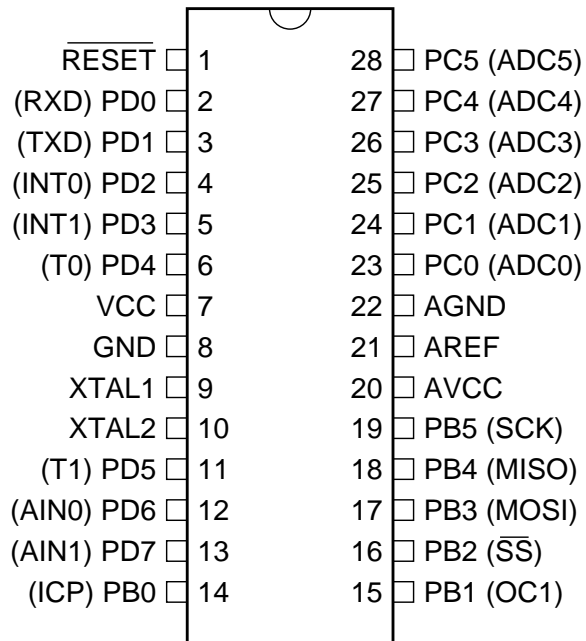
Note: This is a summary document. A complete document is available on our web site at www.atmel.com.

Pin Configurations

TQFP Top View



PDIP



Description

The AT90S4433 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S4433 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S4433 provides the following features: 4K bytes of In-System Programmable Flash, 256 bytes of EEPROM, 128 bytes of SRAM, 20 general purpose I/O lines, 32 general purpose working registers, two flexible Timer/Counters with compare modes, internal and external interrupts, a programmable serial UART, 6-channel, 10-bit ADC, programmable Watchdog Timer with internal Oscillator, an SPI serial port and two software-selectable Power-saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset.

The device is manufactured using Atmel’s high-density non-volatile memory technology. The On-chip Flash Program memory can be re-programmed In-System through an SPI serial interface or by a conventional non-volatile memory programmer. By combining a RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S4433 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

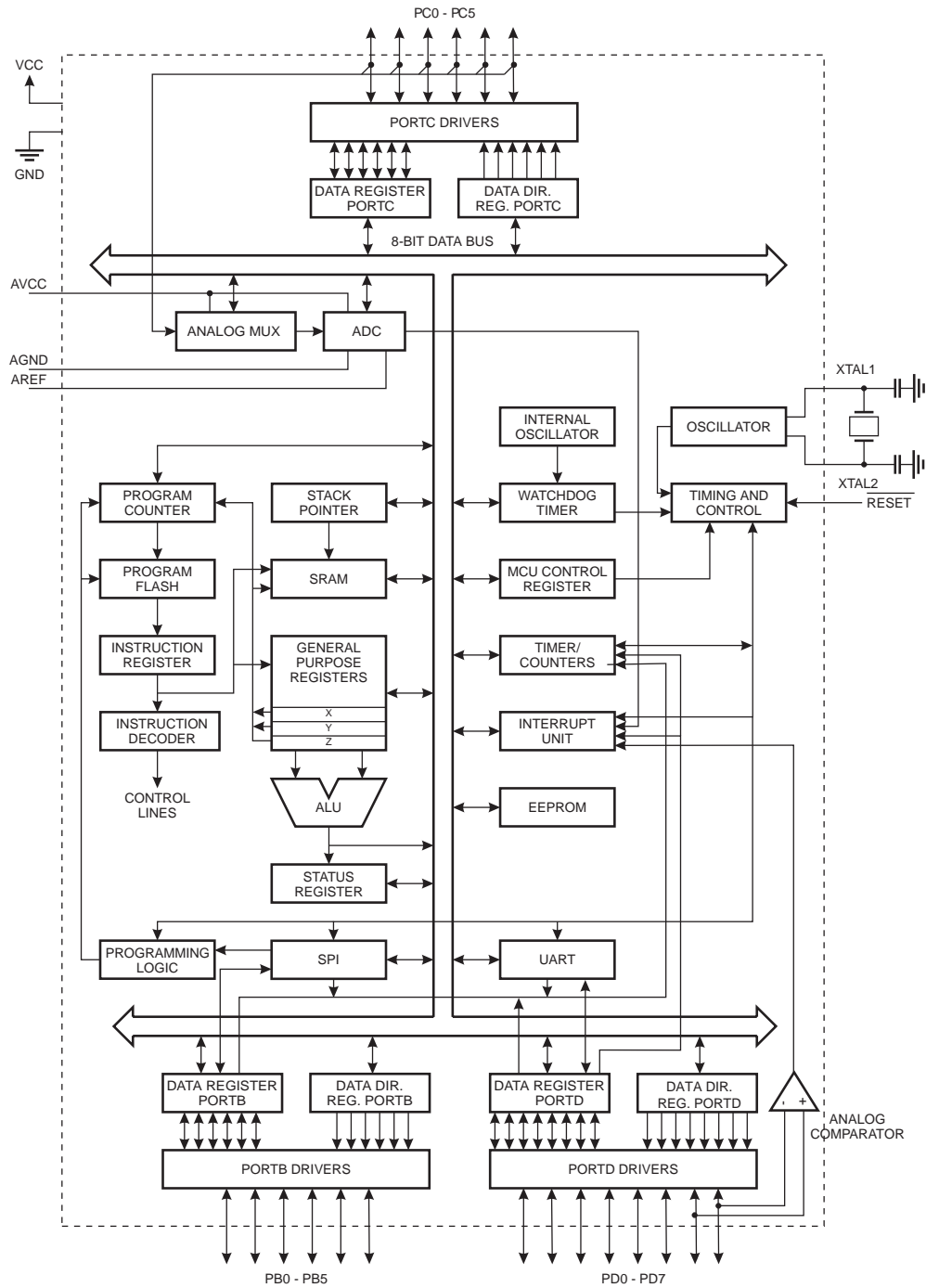
The AT90S4433 AVR is supported with a full suite of program and system development tools including: C Compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators and evaluation kits.

Table 1. Comparison Table

| Device | Flash | EEPROM | SRAM | Voltage Range | Frequency |
|---------------|--------------|---------------|-------------|----------------------|------------------|
| AT90S4433 | 4K | 256B | 128B | 4.0V - 6.0V | 0 - 8 MHz |
| AT90LS4433 | 4K | 256B | 128B | 2.7V - 6.0V | 0 - 4 MHz |

Block Diagram

Figure 1. The AT90S4433 Block Diagram



Pin Descriptions

| | |
|---|--|
| VCC | Supply voltage. |
| GND | Ground. |
| Port B (PB5..PB0) | <p>Port B is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated.</p> <p>Port B also serves the functions of various special features of the AT90S4433 as listed on page 73.</p> <p>The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> |
| Port C (PC5..PC0) | <p>Port C is a 6-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. Port C also serves as the analog inputs to the A/D Converter.</p> <p>The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> |
| Port D (PD7..PD0) | <p>Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.</p> <p>Port D also serves the functions of various special features of the AT90S4433 as listed on page 81.</p> <p>The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.</p> |
| $\overline{\text{RESET}}$ | Reset input. An External Reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. |
| XTAL1 | Input to the inverting oscillator amplifier and input to the internal clock operating circuit |
| XTAL2 | Output from the inverting oscillator amplifier |
| AVCC | AVCC is the supply voltage for Port A and the A/D Converter. If the ADC is not used, this pin must be connected to V_{CC} . If the ADC is used, this pin should be connected to V_{CC} via a low-pass filter. See page 64 for details on operation of the ADC. |
| AREF | AREF is the analog reference input for the A/D Converter. For ADC operations, a voltage in the range 2.0V to AVCC must be applied to this pin. |
| AGND | If the board has a separate analog ground plane, this pin should be connected to this ground plane. Otherwise, connect to GND. |



Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|----------|--|--------|--------|--------|--------|--------|--------|--------|---------|
| \$3F (\$5F) | SREG | I | T | H | S | V | N | Z | C | page 19 |
| \$3E (\$5E) | Reserved | – | – | – | – | – | – | – | – | page 20 |
| \$3D (\$5D) | SP | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | page 20 |
| \$3C (\$5C) | Reserved | – | – | – | – | – | – | – | – | – |
| \$3B (\$5B) | GIMSK | INT1 | INT0 | – | – | – | – | – | – | page 27 |
| \$3A (\$5A) | GIFR | INTF1 | INTF0 | – | – | – | – | – | – | page 27 |
| \$39 (\$59) | TIMSK | TOIE1 | OCIE1 | – | – | TICIE1 | – | TOIE0 | – | page 28 |
| \$38 (\$58) | TIFR | TOV1 | OCF1 | – | – | ICF1 | – | TOV0 | – | page 29 |
| \$37 (\$57) | Reserved | – | – | – | – | – | – | – | – | – |
| \$36 (\$56) | Reserved | – | – | – | – | – | – | – | – | – |
| \$35 (\$55) | MCUCR | – | – | SE | SM | ISC11 | ISC10 | ISC01 | ISC00 | page 30 |
| \$34 (\$54) | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | page 26 |
| \$33 (\$53) | TCCR0 | – | – | – | – | – | CS02 | CS01 | CS00 | page 34 |
| \$32 (\$52) | TCNT0 | Timer/Counter0 (8 Bits) | | | | | | | | page 35 |
| \$31 (\$51) | Reserved | – | – | – | – | – | – | – | – | – |
| \$30 (\$50) | Reserved | – | – | – | – | – | – | – | – | – |
| \$2F (\$4F) | TCCR1A | COM11 | COM10 | – | – | – | – | PWM11 | PWM10 | page 37 |
| \$2E (\$4E) | TCCR1B | ICNC1 | ICES1 | – | – | CTC1 | CS12 | CS11 | CS10 | page 38 |
| \$2D (\$4D) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | page 39 |
| \$2C (\$4C) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | page 39 |
| \$2B (\$4B) | OCR1H | Timer/Counter1 – Output Compare Register High Byte | | | | | | | | page 40 |
| \$2A (\$4A) | OCR1L | Timer/Counter1 – Output Compare Register Low Byte | | | | | | | | page 40 |
| \$29 (\$49) | Reserved | – | – | – | – | – | – | – | – | – |
| \$28 (\$48) | Reserved | – | – | – | – | – | – | – | – | – |
| \$27 (\$47) | ICR1H | Timer/Counter1 – Input Capture Register High Byte | | | | | | | | page 41 |
| \$26 (\$46) | ICR1L | Timer/Counter1 – Input Capture Register Low Byte | | | | | | | | page 41 |
| \$25 (\$45) | Reserved | – | – | – | – | – | – | – | – | – |
| \$24 (\$44) | Reserved | – | – | – | – | – | – | – | – | – |
| \$23 (\$43) | Reserved | – | – | – | – | – | – | – | – | – |
| \$22 (\$42) | Reserved | – | – | – | – | – | – | – | – | – |
| \$21 (\$41) | WDTCR | – | – | – | WDTOE | WDE | WDP2 | WDP1 | WDP0 | page 43 |
| \$20 (\$40) | Reserved | – | – | – | – | – | – | – | – | – |
| \$1F (\$3F) | Reserved | – | – | – | – | – | – | – | – | – |
| \$1E (\$3E) | EEAR | EEPROM Address Register | | | | | | | | page 45 |
| \$1D (\$3D) | EEDR | EEPROM Data Register | | | | | | | | page 45 |
| \$1C (\$3C) | EEDR | – | – | – | – | EERIE | EEMWE | EEWE | EERE | page 45 |
| \$1B (\$3B) | Reserved | – | – | – | – | – | – | – | – | – |
| \$1A (\$3A) | Reserved | – | – | – | – | – | – | – | – | – |
| \$19 (\$39) | Reserved | – | – | – | – | – | – | – | – | – |
| \$18 (\$38) | PORTB | – | – | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 72 |
| \$17 (\$37) | DDRB | – | – | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 72 |
| \$16 (\$36) | PINB | – | – | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 72 |
| \$15 (\$35) | PORTC | – | – | PORTC5 | PORTC4 | PORTC3 | PORTC2 | PORTC1 | PORTC0 | page 78 |
| \$14 (\$34) | DDRC | – | – | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | page 78 |
| \$13 (\$33) | PINC | – | – | PINC5 | PINC4 | PINC3 | PINC2 | PINC1 | PINC0 | page 78 |
| \$12 (\$32) | PORTD | PORTD7 | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | page 80 |
| \$11 (\$31) | DDRD | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | page 80 |
| \$10 (\$30) | PIND | PIND7 | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | page 80 |
| \$0F (\$2F) | SPDR | SPI Data Register | | | | | | | | page 52 |
| \$0E (\$2E) | SPSR | SPIF | WCOL | – | – | – | – | – | – | page 52 |
| \$0D (\$2D) | SPCR | SPIE | SPE | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | page 51 |
| \$0C (\$2C) | UDR | UART I/O Data Register | | | | | | | | page 57 |
| \$0B (\$2B) | UCSRA | RXC | TXC | UDRE | FE | OR | – | – | – | page 57 |
| \$0A (\$2A) | UCSRB | RXCIE | TXCIE | UDRIE | RXEN | TXEN | CHR9 | RXB8 | TXB8 | page 58 |
| \$09 (\$29) | UBRR | UART Baud Rate Register | | | | | | | | page 61 |
| \$08 (\$28) | ACSR | ACD | AINBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | page 62 |
| \$07 (\$27) | ADMUX | – | ADCBG | – | – | – | MUX2 | MUX1 | MUX0 | page 68 |
| \$06 (\$26) | ADCSR | ADEN | ADSC | ADFR | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | page 68 |
| \$05 (\$25) | ADCH | – | – | – | – | – | – | ADC9 | ADC8 | page 69 |
| \$04 (\$24) | ADCL | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 | page 69 |
| \$03 (\$23) | UBRRHI | UART Baud Rate Register High | | | | | | | | page 61 |
| \$02 (\$22) | Reserved | – | – | – | – | – | – | – | – | – |
| \$01 (\$21) | Reserved | – | – | – | – | – | – | – | – | – |
| \$00 (\$20) | Reserved | – | – | – | – | – | – | – | – | – |

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. Some of the Status Flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

Instruction Set Summary

| Mnemonic | Operands | Description | Operation | Flags | # Clocks |
|--|----------|--|---|-----------|----------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add Two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry Two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rdl, K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract Two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry Two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rdl, K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow \$FF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow \$00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd, K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd, K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (\$FF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow \$FF$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd, Rr | Compare, Skip if Equal | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd, Rr | Compare | $Rd - Rr$ | Z,N,V,C,H | 1 |
| CPC | Rd, Rr | Compare with Carry | $Rd - Rr - C$ | Z,N,V,C,H | 1 |
| CPI | Rd, K | Compare Register with Immediate | $Rd - K$ | Z,N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if $(N = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if $(N = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less than Zero, Signed | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half-carry Flag Set | if $(H = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half-carry Flag Cleared | if $(H = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T-flag Set | if $(T = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T-flag Cleared | if $(T = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if $(V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if $(V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if $(I = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if $(I = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move between Registers | $Rd \leftarrow Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |

Instruction Set Summary (Continued)

| Mnemonic | Operands | Description | Operation | Flags | # Clocks |
|--------------------------------------|----------|----------------------------------|--|---------|----------|
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P, b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P, b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n = 0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit Load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Two's Complement Overflow | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Two's Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half-carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half-carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |



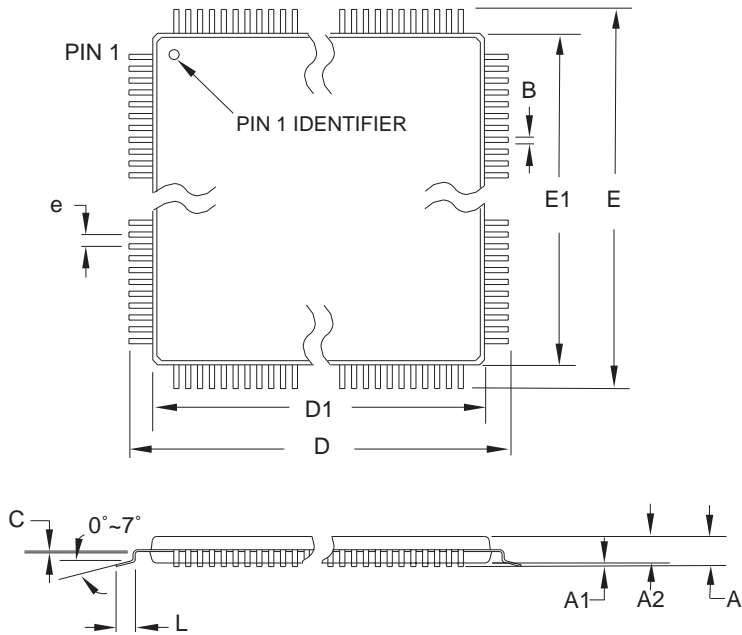
Ordering Information

| Power Supply | Speed (MHz) | Ordering Code | Package | Operation Range |
|--------------|-------------|----------------------------------|-------------|-------------------------------|
| 2.7 - 6.0V | 4 | AT90LS4433-4AC AT90LS4433-4PC | 32A 28P3 | Commercial (0°C to 70°C) |
| | | AT90LS4433-4AI AT90LS4433-4PI | 32A 28P3 | Industrial (-40°C to 85°C) |
| 4.0 - 6.0V | 8 | AT90S4433-8AC AT90S4433-8PC | 32A 28P3 | Commercial (0°C to 70°C) |
| | | AT90S4433-8AI AT90S4433-8PI | 32A 28P3 | Industrial (-40°C to 85°C) |

| Package Type | |
|--------------|--|
| 32A | 32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP) |
| 28P3 | 28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |

Packaging Information

32A



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|------|------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 8.75 | 9.00 | 9.25 | |
| D1 | 6.90 | 7.00 | 7.10 | Note 2 |
| E | 8.75 | 9.00 | 9.25 | |
| E1 | 6.90 | 7.00 | 7.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32A, 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness,
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

DRAWING NO.

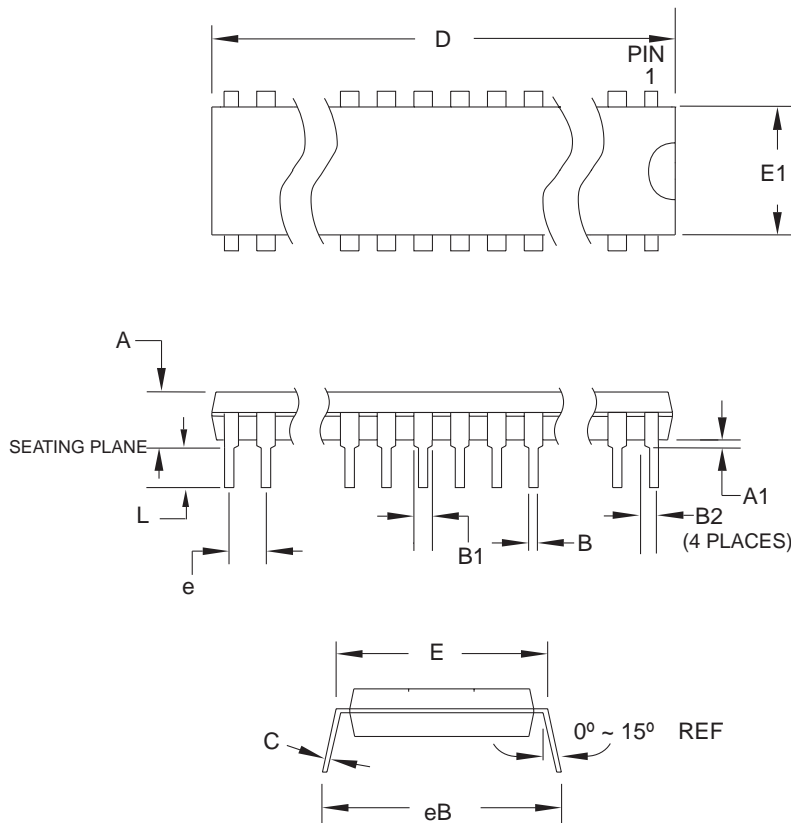
32A

REV.

B



28P3



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | - | - | 4.5724 | |
| A1 | 0.508 | - | - | |
| D | 34.544 | - | 34.798 | Note 1 |
| E | 7.620 | - | 8.255 | |
| E1 | 7.112 | - | 7.493 | Note 1 |
| B | 0.381 | - | 0.533 | |
| B1 | 1.143 | - | 1.397 | |
| B2 | 0.762 | - | 1.143 | |
| L | 3.175 | - | 3.429 | |
| C | 0.203 | - | 0.356 | |
| eB | - | - | 10.160 | |
| e | 2.540 TYP | | | |

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

28P3, 28-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)

DRAWING NO.

28P3

REV.

B

Errata for AT90S/LS4433 Rev. Rev. C/D/E/F

- BOD Keeps the Device in Reset at Low Temperature
- Fuses and Programming Mode
- Incorrect Channel Change in Free Running Mode
- Bandgap Reference Stabilizing Time
- Brown-out Detection Level
- Serial Programming at Voltages below 2.9V
- UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled

7. BOD Keeps the Device in Reset at Low Temperature

When the device operates at low temperature (below 0°C) and the BOD is enabled, the part may fail to start up. At low temperature the BOD may never release the reset, and the part will not start the application. The problem will only occur during start-up and an already running application will not go into reset even if the temperature goes below 0°C.

Note that this also affects the described workaround for Errata no. 4.

Problem Fix/Workaround

If the device operates at low temperature and a BOD is required, an external BOD circuit must be used. Alternatively, ATmega8 can be used instead of AT90S/LS4433.

6. Fuses and Programming Mode

After programming the Fuses in Serial Programming mode, it is not possible to program the Flash or EEPROM. If leaving Programming mode, it is not possible to re-enter Programming mode.

Problem Fix/Workaround

Power the part down and backup again after programming the Fuses or leaving Programming mode.

5. Incorrect Channel Change in Free Running Mode

If the ADC operates in Free Running mode and channels are changed by writing to ADMUX, shortly after the ADC Interrupt Flag (ADIF in ADCSR) is set, the new setting in ADMUX may affect the ongoing conversion.

Problem Fix/Workaround

Use Single Conversion mode when scanning channels, or avoid changing ADMUX until at least 0.5 ADC clock cycles after ADIF goes high.

4. Bandgap Reference Stabilizing Time

The time for the internal voltage reference for the Analog Comparator to stabilize is longer than specified. The stabilizing period starts after the bandgap reference has been selected, and can go on for as much as 10 seconds.

Problem Fix/Workaround

The Bandgap reference will be stable immediately if the internal Brown-out Detector is enabled.

3. **Brown-out Detection Level**

The Brown-out Detection level can increase when there is heavy I/O-activity on the device. The increase can be significant when some of the I/O pins are driving heavy loads.

Problem Fix/Workaround

Select a V_{CC} well above the Brown-out Detection level.
Avoid loading I/O ports with high capacitive or resistive loads.

2. **Serial Programming at Voltages below 2.9V**

At voltages below 2.9V, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 2.9V or higher during In-System Programming.

1. **UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled**

The UART will detect a UART start bit and start reception even if the UART is not enabled. If this occurs, the first byte after reenabling the UART will be corrupted.

Problem Fix/Workaround

Make sure that the RX line is high at start-up and when the UART is disabled. An external RS-232 level converter keeps the line high during start-up.

**Data Sheet
Change Log for
AT90S/LS4433**

This section contains a log on the changes made to the data sheet for AT90S/LS4433. All references to pages in Change Log, are referred to this document.

**Changes from Rev.
1042E-09/01 to Ref.
1042F-03/02**

- 1 Updated minimum AREF Voltage on page 5 and page 64.
- 2 Corrected VBOT Max for BODLEVEL = 1 in Table 4 on page 22.
- 3 Updated Corporate Template.

**Changes from Rev.
1042F-03/02 to Ref.
1042G-09/02**

- 1 Added watermark "Not recommended for new designs. Use ATmega8".
- 2 Added Errata Sheet to the Data Sheet.

**Changes from Rev.
1042G-09/02 to Ref.
1042H-04/03**

- 1 Updated the "Errata for AT90S/LS4433 Rev. Rev. C/D/E/F" on page 13.
- 2 Updated "Packaging Information" on page 11.



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